AARUSH KUMBHAKERN

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RESEARCH SUMMARY

Final-year B.Sc. (Hons.) student at Ashoka University, working in program analysis and software reliability — principally grammar-based fuzzing, delta debugging, and the reduction of failure-inducing inputs. Recent work preserves the 1-minimality guarantees of classical delta debugging at a fraction of its oracle cost. Adjacent work includes a statically verifiable instruction set for programmable microfluidics and a pipeline that translates natural-language procedures into structured representations. Applying for doctoral study in program analysis and software reliability.

Research interests

- Program analysis
- Software reliability
- Grammar-based fuzzing
- Delta debugging & reduction
- Compilers & DSLs
- Static program reasoning

EDUCATION

Ashoka University Sep. 2022 – Dec. 2026 (expected)
B.Sc. (Hons.), Four-Year with Research in Computer Science; Minor in Biology *Sonipat, India*
CGPA: 3.63 / 4.00

Undergraduate thesis: *A Formally Verifiable Programmable Microfluidic Architecture Using Two-Phase Slug Flow*

Selected coursework: Theory of Computation; Programming Languages and Translation; Computer Organization and Systems; Design and Analysis of Algorithms; Numerical Algorithms and Optimization; Information Security; Computer Networks; Probability and Statistics; Reinforcement Learning; Machine Learning. *Biology (minor):* Physiology, Cell Biology, Chemical Basis of Life, Force and Motion in Biology (biomechanics), Smart and Biomaterials.

PUBLICATIONS

Refereed publications

Aarush Kumbhakern and Bhargab B. Bhattacharya. "HyDRA: A Slug-Flow Microfluidic Architecture and Instruction Set." To appear in *Proc. IEEE Computer Society Annual Symposium on VLSI* (ISVLSI), Kolkata, India, July 2026 (oral presentation).

Aarush Kumbhakern, Saransh Kumar Gupta, Lipika Dey, and Partha Pratim Das. "Towards an Action-Centric Ontology for Cooking Procedures Using Temporal Graphs." In *MMFood '25: Proceedings of the 1st International Workshop on Multi-modal Food Computing* (co-located with ACM Multimedia 2025), Dublin, Ireland, Oct. 2025. ACM. doi:10.1145/3746264.3760499

Under review

Aarush Kumbhakern, Xi Wu, Feiyang Chen, Danushka Liyanage, and Rahul Gopinath. "Dr. DD: 1-Minimal Isolation of Failure Causes via Deferred Restarts." Under major revision, *IEEE International Symposium on Software Reliability Engineering* (ISSRE), 2026.

RESEARCH EXPERIENCE

University of Sydney Nov. 2023 – Present
Visiting Research Student | Advisor: Prof. Rahul Gopinath *Sydney, Australia (remote)*

Fuzzing, delta debugging, and input reduction.

- Designed and built the experimental harness and full empirical evaluation of `drdd`, a structure-agnostic drop-in replacement for `ddmin` that preserves its 1-minimality guarantee while deferring restarts to the single-element level; measured a 2–60× reduction in oracle calls across four input formats (ffmpeg, XML, binutils, crashjs) at matching reduction quality. First-author paper under major revision at ISSRE 2026. [dd-lab]
- Built grammar-based fuzzers in C and compiler-style tooling that generates them from grammar specifications, iterating on profiling and low-level implementation design for performance. [fuzzer]

· Current direction: inferring acceptance grammars from `ddmin` runs to generate minimal inputs.

Undergraduate Thesis — HyDRA, Ashoka University Aug. 2025 – May 2026
Researcher | Advisor: Prof. Bhargab B. Bhattacharya *Sonipat, India*

A Formally Verifiable Programmable Microfluidic Architecture Using Two-Phase Slug Flow.

· Recast a sample-preparation capstone as an architecture-and-abstraction problem: designed HyDRA, a programmable slug-flow microfluidic substrate with a single-static-assignment, integer-valued ISA over discrete fluid operations, plus its microarchitecture and physical architecture.

· Specified a finite-state chip abstraction whose safety properties reduce to Boolean combinations of integer linear inequalities — decidable ahead of time in polynomial resources.

· Framed the result as a programmable, statically verifiable substrate (architecture + ISA + static guarantees); accepted at ISVLSI 2026.

Mphasis AI & Applied Tech Lab May 2025 – Present
Undergraduate Researcher, Food Computing | Advisor: Prof. Partha Pratim Das *Sonipat, India*

Recipe DSL and LLM-based pipeline.

· Designed a domain-specific language that models cooking procedures as action graphs — ingredients, intermediate components, transformations, dependencies, and procedural branches — turning loose natural-language recipes into structured computational objects; published at MMFood '25.

SYSTEMS & ENGINEERING EXPERIENCE

Catalis Packaging Technologies Pvt. Ltd. Oct. 2023 – Jan. 2024
Engineering Intern *Vadodara, India*

· Built a suite of interconnected Linux/`systemd` services and daemons on Raspberry Pi-class hardware — a USB-triggered automated workflow for industrial HMIs, with machine telemetry collected over Modbus and streamed to the cloud — owning the end-to-end architecture and operational reliability. [cloud-hmi]

AWARDS

· Best Undergraduate Thesis, Department of Computer Science, Ashoka University (2026).
· UToronto Engineering International Scholar Award (entrance scholarship, CAD $140,000), 2022; declined.

TEACHING

Lodha Genius Program, Ashoka University May – Jun. 2025
Teaching Assistant *Sonipat, India*

· Mentored five students one-on-one in data interpretation and simulation development for an intensive one-month course on computational modeling and biological-systems analysis.

TECHNICAL SKILLS

Programming	C, Python, JavaScript
Systems & tooling	Linux, `systemd`, Git, Make, Modbus, profiling & benchmarking, experimental harnesses
Methods & areas	Compilers & DSLs, program analysis, fuzzing, delta debugging & input reduction, empirical evaluation, finite-state modeling & static reasoning, scheduling & optimization, embedded & cyber-physical systems, machine learning

REFERENCES

References available on request.